(19) Europäis hes Pat ntamt
European Patent Office
Offic uropéen des br v ts

(11) EP 1 179 852 A2

(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
13.02.2002 Bulletin 2002/07

(51) Int Cl.[7]: **H01L 27/146**, H01L 31/0224

(21) Application number: **01306424.1**

(22) Date of filing: **26.07.2001**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **03.08.2000 US 632106**

(71) Applicant: **GENERAL ELECTRIC COMPANY**
Schenectady, NY 12345 (US)

(72) Inventors:
- **Kwasnick, Robert Forrest**
Paso Alto, California 94303 (US)
- **Possin, George Edward**
Niskayuna, New York 12309 (US)
- **Wei, Ching-Yeu**
Niskayuna, New York 12309 (US)

(74) Representative: **Pedder, James Cuthbert et al**
GE London Patent Operation, Essex House,
12/13 Essex Street
London WC2R 3AA (GB)

(54) **Solid state imager having gated photodiodes and method for making same**

(57) A solid state imager is provided that comprises an imaging array of gated photodiodes. The imager comprises a plurality of photosensor pixels arranged in a pixel array, and each of the photosensor pixels includes a photodiode having a sidewall, the sidewall having a gate dielectric layer disposed thereon, and a field plate disposed around the photodiode body. The field plate comprises amorphous silicon disposed on the gate dielectric layer and extends substantially completely around the sidewall of said photodiode. The field plate is electrically coupled to the common electrode of the imaging array so that the field plate creates an electric field around the photodiode body in correspondence with the potential of said common electrode. A method of fabricating the gated photodiode array is also provided.

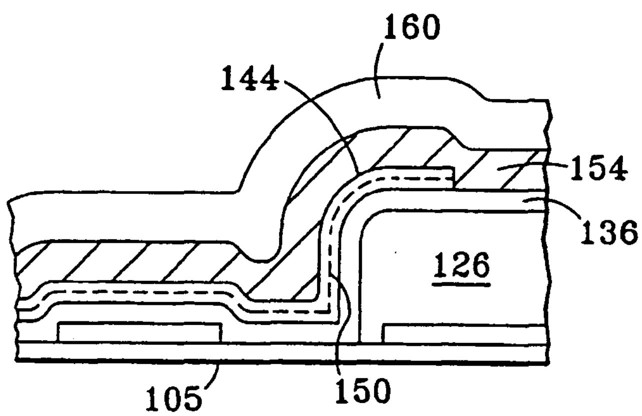

FIG. 4

EP 1 179 852 A2

D scription

[0001] The invention relates generally to larg area solid state imager devices and specifically to imager devices having reduced photodiode sidewall leakage.

[0002] Solid state imager devices are used for radiation imaging (e.g., x-rays), such as for use in medical diagnostics. Such solid state imager devices commonly comprise arrays of photosensor elem nts with associated switching elements arranged in rows and columns, with the photosensor elements being addressed by rows of scan lines (also referred to as address lines) and columns of data lines (also referred to as read-out lines). Typically, the photosensor elements are photodiodes, and the switching elements are thin film field effect transistors (FETs or TFTs).

[0003] One of several factors that can influence solid state imager performance is the amount or level of photodiode reverse bias leakage. In the solid state imager devices to which the present invention is directed, the photodiode leakage is regarded as having two components, sidewall leakage (from surfaces of the photodiode with substantial incline to the substrate) and area leakage (from photodiode surfaces substantially parallel to the substrate).

[0004] In imager devices to be used in medical applications, the photodiodes in a representative pixel typically have approximately square dimensions on the order of about 0.1 to 0.4 mm in length and width. At such sizes, the sidewall leakage component is of the same order of magnitude as the area leakage component; thus both components contribute significantly to the leakage, thereby degrading the performance of the imager. For example, in radiographic applications, the exposure time (between read outs of the array) can be as long as two (2) seconds, and a photodiode leakage of even 1 pA will degrade performance significantly by saturation of the charge that the photodiode is able to collect, and by contributing to imager noise and offset drift associated with the leakage current.

[0005] The potential severity of the photodiode leakage problem is best appreciated when it is considered that the photodiodes may operate under about 10V common bias, at a temperature somewhat above room temperature due to heat generated by surrounding electronic components. Further, the imager device may have on the order of one million (1×10^6) photodiodes, of which a high percentage must not be leaky in order to avoid having an excessive number of bad pixels. It is therefore desirable to reduce the reverse bias leakage of the imager photodiodes to the extent practicable, while avoiding an increase in the cost and/or complexity of the imager fabrication process, and while avoiding any degradation in performance or reliability.

[0006] In one embodiment of the invention, a solid state imager is provided that comprises an array of gated photodiodes. The imager comprises a plurality of photosensor pixels arranged in a pixel array, and each of the photosensor pixels includes a photodiode having a side wall, the sidewall having a gate dielectric layer disposed thereon, and a field plate disposed around the photodiode body. The filed plate comprises amorphous silicon disposed on the gate dielectric layer and extends substantially completely around the sidewall of said photodiode. A method of fabricating the gated photodiode array is also provided.

[0007] The invention will now be described in greater detail, by way of example, with reference to the drawings, in which:-

Figures 1A-D are substantially schematic top plan views of a representative photosensor pixel of the present invention at the various steps of a production process.

Figures 2A-D are substantially schematic cross-sectional views taken along the noted section lines in Figures 1A-D, respectively.

Figures 3A-D are substantially schematic cross-sectional views taken along the noted lines in Figures 1A-D, respectively.

Figures 4 and 5 are substantially schematic cross-sectional views of the device illustrated in Figure 2D and 3D, respectively, with a final barrier layer deposited over the exposed surfaces of the photosensor pixel of the present invention.

Figure 6 is a substantially schematic top plan view of a representative photosensor pixel in accordance with a further embodiment of the present invention.

Figure 7 is a substantially schematic cross-sectional view taken along section line 7-7 in Figure 6.

Figure 8 is a substantially schematic cross-sectional view taken along section line 8-8 in Figure 6.

Figure 9 is a substantially schematic cross-sectional view of a representative photodiode island in accordance with the present invention.

Figure 10 is a graph presenting xperimental data illustrating a decr ase in diode leakage employing a device in accordance with th present inv ntion.

Figure 11 is a plan view of th imager array showing a plurality of representative pixels and with respective photoresist TFT apertures;

[0008] A radiation imager 100 (Figure 11) fabricated in accordance with the present invention comprises a plurality of gated photodiodes. The term "imager", as used herein, refers to a solid state device that is adapted to absorb incident radiation of a particular wavelength (such as optical photons, x-rays, or the like) and to generate an electrical signal corresponding to the absorbed radiation. As is known in the art, typically the pixels are disposed in an array having a pattern of rows and columns. As each pixel 110 is individually addressable by respective rows of scan lines and columns of data lines, the spatial distribution of radiation absorbed by the array is also determinable. The photosensor array is electrically coupled to electrical circuits (not shown) situated off of the substrate. Those circuits amplify and process the electrical signals generated by the array.

[0009] As an example, an array of such pixels may be a light imaging array (e.g., an array of photosensors such as photodiodes), and can be employed as an x-ray imager by coupling the light imager array to an x-ray scintillator (which comprises a material that emits optical photons when the x-ray radiation (or other type of radiation being detected) is absorbed in the scintillator).

[0010] "Gated photodiodes" as used herein refers to diode assemblies in which have a band (or belt) of semiconductive material disposed around the sidewalls of the photodiode body so as to provide a "field plate", or means, when in operation, of establishing an electrical field around the diode body so as to reduce electrical leakage from the sidewalls of the diode in the array. The belt of semiconductive material disposed around the diode body sidewalls (with dielectric material disposed between the diode body and the belt of semiconductive material) is typically electrically coupled to the anode of the diode. This arrangement forms a "field plate" or "gated" diode structure that reduces diode leakage.

[0011] A number of processes exist by which photosensor arrays can be fabricated; it is desirable that fabrication processes provide not only components in the array that deliver desired performance but also that the fabrication steps be efficient from a time and resource standpoint. By way of example and not limitation, the imager devices described herein are produced by what is referred to as a reduced mask set imager process, one aspect of which is that the photodiode bodies (comprising the semiconductive material of the diode) for the respective pixels are deposited prior to the deposition of the associated thin film transistors. The solid state imager of the present invention, which has decreased reverse bias current leakage, is fabricated in steps, with the resultant structures from identified steps being illustrated in Figures 1A-D, and in corresponding cross-section views 2A-D and 3A-D. The reduced mask fabrication method is discussed generally in U.S. Patents 5,399,844; 5,435,608; and 5,480,810; all of which are assigned to the assignee herein. The present invention provides modifications to the process to achieve the pixel configuration resulting in the reduction in reverse bias leakage of the photodiodes.

[0012] For purposes of illustration and not limitation, a representative pixel 110 is illustrated in the figures herein and the accompanying description refers to such a representative pixel. Pixels 110 are typically disposed on a substrate 105 (Figures 1A-1D). Each pixel 110 comprises a photosensor, such as photodiode 126, as shown and described herein, and a switching device such as a thin film field effect transistor (FET), also referred to as a TFT. Typically, in accordance with known fabrication processes, fabrication of all pixels on a substrate 105 that will form a particular imager photosensor array proceeds simultaneously.

[0013] In accordance with the method of the invention, a first conductive layer 120 is deposited on a surface of substrate 105 (a portion of first conductive layer 120 remaining after etching is illustrated in Figures 1A, 2A, 3A). A gate electrode 122 and photosensor bottom gate electrode 124 are formed in a common etching sequence by etching first conductive layer 120 in accordance with a pattern, such as is defined by an appropriately patterned photoresist mask, conforming to the desired positioning of the gate electrode 122 and the bottom electrode 124. As used herein, the term "common etching sequence" and similar terms refer to the coincident formation of components in the pixel, such as etching the underlying material to be formed into respective components, in one set of etching steps through one patterned photoresist mask.

[0014] The conductive layer 120 from which gate electrode 122 and photosensor bottom electrode 124 is formed typically comprises indium-tin-oxide (ITO), or a metal such as chromium, titanium, molybdenum, aluminum, or the like, deposited in one or in multiple layers to a thickness on the order of 100 Angstroms to 10,000 Angstroms.

[0015] After gate formation, the photodiode island 126 is formed (Figure 1B, 2B, 3B; the portion of diode bottom electrode underlying the diode island 126 is illustrated in phantom). The photodiode island 126 typically comprises three layers (illustrated with broken lines in cross-sectional Figures 2B and 3B) of amorphous silicon (a-Si), with an n-type doped amorphous silicon layer 128 deposited first, followed by an undoped amorphous silicon layer 130, also referred to as intrinsic amorphous silicon (i-Si) and then a p-type doped amorphous silicon layer 132. The representation

in Figures 2B and 3B are for purposed of illustration only; typically the n-type and p-type layers are thinner than th undoped amorphous layer. In addition, the photodiode island may have a thin layer of conductive transparent material such as indium tin oxide (ITO) disposed across the upper surface 133 of the photodiod . Th layer of ITO is not shown in the Figures, in order to simplify the illustration of the device. Th preferr d thickness of th photodiode island 126 is in the range of about 0.5μm to about 2.5μm.

[0016] As with conductive layer 120, the layers making up photodiode island 126 are initially deposited substantially uniformly across the substrate 105, and the gate electrodes 122 and bottom electrodes 124 situated thereon. The photodiode islands are then formed by etching through silicon layers 132, 130, 128, to expose the gate electrode 122, with the island being formed (see Figure 1B) over all but a small contact portion 123 of bottom electrode 124.

[0017] In the present invention, the etching of the photodiode island material is done so as to render the photodiode sidewalls 134 substantially vertical (e.g., desirably disposed at an angle with respect to substrate surface 105 of about 85 to about 90 degrees), as is practicable within economic and technological constraints. It is especially desired that the sidewall 134 be formed having at least a portion thereof oriented substantially vertically. This may be achieved by a reactive ion etching (RIE), for example with SF_6 or HCl 20 sccm/30 sccm, at 1.6 W/cm^2 and 13.56 MHz, and at a pressure of about 100 mTorr to about 80 mTorr.

[0018] As a practical matter, it is extremely difficult with current etching technologies, to obtain a completely vertical sidewall 134 on the photodiode island 126. Figure 9 and associated Table I below provide examples of contour and orientation of portions of the sidewalls 134 that are reasonably attainable with a 1.5 micron thick diode island using the reactive ion etching of the present invention. The verticality of sidewall 134 resulting from this process is determined partly by the slope of the patterning photoresist; the post-bake of the resist required after resist pattern delineation is done so that the resist is not excessively cross-linked during RIE (which may make the resist to difficult to remove subsequent to RIE) and tends to make the resist profile less vertical.

TABLE I

(1.5 micron thickness diode island)				
RIE Pressure (mT)	bottom slope S1 (approx. deg)	middle slope S2 (approx. deg)	extent of middle region E (approx. microns)	top slope S3 (approx. deg)
100	75°	90°	0.37 to 0.67	77°
80	80°	85° to 90°	0.37	77°
60	76°	no middle region	no middle region	67°
50	75°	no middle region	no middle region	64°

[0019] It can be seen from Table I that the use of pressures lower then about 80 mTorr yield a sidewall having no substantially vertical portion, but only a sloping sidewall which decreases in steepness from the lower (S1) to the upper (S3) end. In contrast, the use of a pressure of 80-100 mTorr produces an intermediate section S2 of the sidewall which is substantially vertical, that is, oriented on the order of 85°-90° to the substrate surface (referring to the direction of perpendicular or orthogonal to the surface of the substrate. It can further be seen that, at the higher 100 mTorr pressure, the intermediate section S2 is more vertical/orthogonal and extends over a greater portion of the height of the sidewall, than does the intermediate section S2 formed using 80 mTorr as the RIE pressure.

[0020] Following the formation of the photodiode 126, the thin film transistor (TFT) deposition and patterning is performed, as illustrated in Figures 1C and D; 2C and D; 3C and D. Commonly, in a plasma-enhanced chemical vapor deposition (PECVD) process, multiple layers of material are deposited that are then patterned to provide the desired component structure on the array. For example, a gate dielectric layer 136 is deposited first, which layer typically comprises one or more layers of silicon nitride, silicon oxide, or combinations thereof, and is deposited at a thickness in the range of about 0.1-0.5 microns.

[0021] Additionally, materials 138 to form thin film transistor (TFT) 175 (Figure 1D) are deposited in the PECVD process. The TFT 138 commonly comprises an inverted-staggered TFT, having two PECVD silicon layers (see Figure 2C), a first layer 140 of which is intrinsic amorphous silicon (i-Si) in a thickness of about 0.1 μm to 0.3μm. The second or top layer 142 of TFT 138 commonly comprises n^+-doped Si (n^+-Si) of a thickness less than about 0.1μm. In Figure 2C, layer 138 is shown after the patterning step described below. As is known in the art, a thin metal capping layer (not shown) of, for example, Mo or Cr, may optionally be formed on the top of second layer 142 of TFT 138.

[0022] As is the case in the known standard reduced mask set process, the next step is to form TFT/FET islands 144, 146 (see Figure 1C) at desired locations, by removing the deposited TFT-silicon material from other areas on the pixel 110. As used herein, "TFT material silicon material" and the lik refer to the semiconductive portion of the TFT, illustrated in the Figures generally as item 138. This selective TFT silicon material removal is typically achieved using

an etching procedure. In the process of the pr sent invention, this etching step is conducted so as to remove the TFT material from the horizontal (that is, parallel to substrate) planar surfaces of the pixel, but to avoid removing, or to remove only a portion of, the TFT silicon material disposed on the substantially vertical sidewall portions 134, of the photodiode 126, so as to form a spacer (or b lt) 150 forming a belt-like lay r of silicon around the photodiode body sidewalls.

[0023] In order to accomplish this, a reactive ion etch, or dry etch is employed, using, for example, a SF_6/HCl 20 sccm/30 sccm etchant, at 1.1 W/cm^2 and 13.56 MHz, with a pressure of about 100 mTorr. The etching is performed to an emission endpoint, for example, based on a Si line at 288 nm, plus a few minutes (typically determined empirically), generally about one to three minutes. If the etching time is too short, residual silicon material remains along the gate steps or on the field (other horizontal surfaces) of the array, leading to inter-pixel leakage. If the etching time is too long, the underlying gate dielectric material can be etched away, which can also cause leakage in the array, and prolonged etching can also result in etching away of the silicon material that forms field plate (or belt spacer) 150.

[0024] This etching procedure results in the TFT silicon material being removed from the desired horizontal surfaces while leaving intact the field plate (or belt spacer) 150 of the TFT silicon material (i.e., an a-Si material) around the perimeter of the photodiode 126, on the substantially vertical sidewalls 134 of the photodiode body. The etching process will typically etch off the upper n$^+$-doped Si material from the vertical photodiode sidewalls 134, and thus the layer of silicon forming field plate 150 typically comprises only the i-Si portion of the initially deposited TFT material, which material extends in a continuous belt around the sidewalls of photodiode body 126. The gate electrode dielectric layer 136 is disposed between field plate 150 and the sidewall of the photodiode 126, thus leaving the silicon of field plate (or spacer) 150 electrically isolated from diode body so that the gated diode structure of the present invention can be formed.

[0025] The formation of field plate (or belt spacer) 150 on the sidewall of photodiode 126 is made possible by the order of steps employed in a reduced mask set process, in particular, because the photodiode is formed prior to forming the TFT islands in the reduced mask set process.

[0026] Subsequent to the formation of the TFT/FET islands 144, 146 and field plate (or belt spacer) 150, the device fabrication process continues by forming vias 152 in the gate dielectric layer, followed by the deposition and patterning of a source/drain metal layer (source/drain metal refers to the common material used to form both the source and drain electrodes in the TFT), which is patterned to form common electrode lines 154 and other contacts 155 (that comprise, for example, the source and drain electrodes of the TFT and the readout line coupled to the TFT. The source/drain metal layer typically is a conductive material such as molybdenum, chromium, or the like.

[0027] As seen in Figure 2D, the common electrode lines 154 overlap the sidewalls of the photodiode islands at regions in the vicinity of TFT island structures 144. In operation, the common electrodes are generally held at a fixed potential. Since the common electrode 154 contacts the a-Si material of field plate (or belt spacer) 150, which is slightly conductive, the silicon in belt 150 charges up to the bias of the common electrode. The electric field provided by the field plate 150 results in a reduction, in operation, of reverse bias leakage from the photodiode 126. Furthermore, if the common electrode is negatively biased, as is the case with p/i/n-type photodiodes (top to bottom layers, as seen in Figures 2B, 3B), then the potential of the field plate 150 silicon material is negative with respect to the more positive potential of the body of diode 126 and a highly conductive FET channel charge layers forms in the silicon of belt spacer 150. This situation significantly increases the conductivity of the silicon field plate enhancing the field on the diode sidewall.

[0028] In final processing, additional material is removed from regions of the TFT/FET islands 144, 146 that are not covered in source/drain metal. This step removes the n+-Si layer and a small amount of the underlying i-Si layer, so that about 50 nm to about 100 nm of the n$^+$-Si and i-Si are removed in total; the purpose of this removal is to create a functioning TFT, as is known in the art. Reactive ion etching is the preferred procedure because the material is etched substantially orthogonally to the surface, and thus will not remove, or will remove only a slight amount of, the spacer material 150 along the sidewall 134 of the photodiode. The reactive ion etch may preferably employ SF_6 and HCl, as in prior etching steps. If desired or necessary, an additional photoresist masking layer (not shown) can be used at this step to protect the field plate (or belt spacer) 150 material on the diode sidewalls while allowing the n+ layer 142 to be removed from the FET channel 170. The photoresist masking layer is disposed over the array with respective pixel apertures disposed to allow the etching of the silicon material in the channel regions 170.

[0029] The imager is then completed by the deposition of a barrier layer 160 (Figures 4 and 5), which passivates the surface of the TFT/FET islands 144, 146, and seals the exposed surfaces of the entire device. The barrier layer is preferably about 0.5 μm to about 2.0 μm in thickness, and may preferably comprise SiO_x SiN_x, or combinations thereof. Figure 11 shows a plan view of the imager array 100 with respective photoresist TFT apertures 165 ov r th TFT regions to allow etching of the channel 170.

[0030] Figures 6, 7 and 8 illustrate an alternative embodiment of the present invention, produced by using standard photolithography in the step in which the TFT/FET islands 244, 246, are initially formed. When using photolithography, TFT island 244 typically is patterned such that the island remains around the perimeter of the photodiode 226, over-

lapping (see Figure 7) the upper planar surface 248 of the photodiode, which has the layer of gate dielectric material 236 deposited thereon. This overlap of material decreases the photoresponse or sensitivity of the photodiode 226 to a certain d gree, however, it also results in a wider or thicker layer of the a-Si mat rial to act as the sidewall field plate (or belt spacer) 250 to provide the gated diode structure. As compared with the us of RIE to etch the TFT/FET islands in the previous embodiment, th use of photolithography provides a more reliable method for leaving the Si material on the sidewall.

[0031] Figure 10 is a graph which shows experimental data, obtained in connection with the development of an experimental gated diode structure of the present invention, evidencing a decrease in reverse bias leakage in a device having a field plate (or belt) 150 extending along the sidewall of the photodiode. In the gated diode device used in generating the data presented in Figure 10, the gate electrode material employed was indium tin oxide (ITO), and the gate dielectric was silicon nitride, at a thickness of about 0.1 micron. The device was constructed so that a separate bias could be applied to the gate. In the invention the gate electrode is electrically connected to the bias electrode.

[0032] Without the gate (V_g about 0V) the leakage current in the experimental example would be about 10^{-9} A. With the gate tied to V_{bias} about -8V, the leakage would be about 10^{-12} A (i.e., $V_{gate} = V_{bias} = -8V$).

[0033] For the sake of good order, various aspects of the invention are set out in the following clauses:-

1. A solid state imager comprising:
   a plurality of photosensor pixels arranged in a pixel array, each of said photosensor pixels comprising:

   a photodiode having a side wall, said sidewall having a gate dielectric layer disposed thereon; and
   a field plate disposed around said photodiode body, said field plate comprising amorphous silicon disposed on said gate dielectric layer, said field plate extending substantially completely around said sidewall of said photodiode.

2. The solid state imager of Clause 1 wherein said imager further comprises a common electrode, said field plate being disposed in electrical contact with a portion of said common electrode.

3. A solid state imager as recited in Clause 2, wherein said photodiode sidewall is disposed substantially perpendicular with respect to a surface of a substrate on which said pixel array is disposed.

4. A solid state imager as recited in Clause 3 wherein said field plate is disposed over the substantially perpendicular portion of said photodiode sidewall.

5. A solid state imager as recited in Clause 1 wherein said amorphous silicon material of said field plate extends over said photodiode sidewall and at least a portion of the upper surface of said photodiode body.

6. A solid state imager as recited in Clause 5, wherein said photodiode is selected from the group consisting of p-I-n diodes and n-i-p diodes.

7. A method of fabricating an imager array having a plurality of pixels, each pixel comprising a respective pixel thin film transistor and a pixel photosensor, the method comprising, for each respective pixel, the steps of:

   depositing a first conductive layer on a substrate;
   forming a photosensor bottom electrode from said first conductive layer;
   forming a photosensor body disposed on at least a portion of said photosensor bottom electrode, said photosensor body having sidewalls;
   depositing a gate electrode dielectric layer over said photosensor body;
   forming a layer of field plate comprising amorphous silicon on at least a portion of said gate dielectric layer covering said sidewall of said photosensor body and extending completely around said photosensor body; and
   forming a common electrode in electrical contact with said field plate.

8. The method of Clause 7, wherein the step of forming said common electrode further comprises:

   depositing a source/drain conductive material;
   patterning said source/drain conductive material to form said common electrode and to form a source electrode and a drain electrode for a thin film transistor (TFT) for each of said pixels.

9. The method of Clause 7, further comprising the step of forming an island of TFT material following deposition

of said gat electrode dielectric layer, comprising th steps of:

depositing a first layer of intrinsic amorphous silicon over substantially an entir exposed surface of said gat dielectric material;
depositing a second layer of n^+-doped amorphous silicon material over said layer of intrinsic amorphous silicon; and
etching said first and second layers to substantially remove said first and second layers from predetermined portions of said gate dielectric layer disposed so as to leave said first and second layers in selected area where said TFT islands are to be present, and further leaving intact at least a portion of said first layer of amorphous silicon on said sidewall of said photosensor body.

10. The method of Clause 9, wherein said etching step comprises a reactive ion etch.

11. The method of Clause 10, wherein said reactive ion etch employs an etchant of SF_6 or HCl.

12. The method of Clause 11, wherein said reactive ion etch includes etching with 20 sccm/30 sccm mixture of SF_6 or HCl, at 1.1 W/cm^2 and 13.56MHz, a pressure of about 100 mTorr, wherein the etching is conducted at an emission endpoint of silicon, plus about one to three minutes so as to form said field plate.

13. The method of Clause 9, wherein said etching step is carried out using photolithography.

14. The method of Clause 7, wherein the step of forming said photosensor body further comprises forming a substantially orthogonal side wall portion, comprising the steps of:
depositing substantially uniform layers of, in succession, an n^+-doped amorphous silicon, an intrinsic amorphous silicon, and a p^+-doped amorphous silicon, and etching said layers at predetermined locations using a reactive ion etch employing a 20 sccm/30 sccm mixture of SF_6/HCl, at 1.6W/cm^2, and 13.56 MHz, at a pressure between about 80 mTorr and 100 mTorr, to form a photodiode having said substantially vertical sidewall portion extending completely around said photodiode.

15. A radiation imager comprising:

a substrate;
a photosensor array disposed on said substrate, said photosensor array comprising a plurality of pixels, each of said pixels being coupled to a scan line and a data line, each of said pixels further comprising:

a photodiode having a body with sidewalls;
a thin film transistor (TFT), said TFT being electrically coupled to said photodiode and said scan line and data line so as to enable selective readout of the charge of said photodiode;
a common electrode disposed in electrical contact with said photodiodes; and
a field belt comprising amorphous silicon disposed around said photodiode sidewalls with a dielectric material being disposed between said field plate and said photodiode body, said field belt being in electrical contact with said common electrode so as to provide an electric field around said photodiode body in correspondence with the potential of said common electrode.

16. The radiation imager of clause 15 wherein said common electrode, at points where it is disposed over the sidewalls of said photodiode bodies, is disposed over respective TFT islands, said TFT islands comprising silicon materials used in the TFT fabrication process.

17. The radiation imager of clause 16 wherein said photodiode body sidewalls over which said field plate extends comprise a portion that is substantially vertical to the surface of said substrate.

18. The radiation imager of clause 17 wherein said substantially vertical sidewalls are disposed at an angle between about 85 and about 90 degrees with respect to the surface of said substrate.

19. The radiation imager of clause 15 wherein said photodiode is selected from the group consisting of p-i-n diodes and n-i-p diodes.

20. The radiation imager of clause 15 wherein said field plate comprises silicon selected from the group of intrinsic

amorphous silicon, n+ doped silicon, and combinations thereof.

Claims

1. A solid state imager comprising:
   a plurality of photosensor pixels arranged in a pixel array, each of said photosensor pixels comprising:

   a photodiode having a side wall, said sidewall having a gate dielectric layer disposed thereon; and
   a field plate disposed around said photodiode body, said field plate comprising amorphous silicon disposed on said gate dielectric layer, said field plate extending substantially completely around said sidewall of said photodiode.

2. The solid state imager of Claim 1 wherein said imager further comprises a common electrode, said field plate being disposed in electrical contact with a portion of said common electrode.

3. A solid state imager as recited in Claim 1 or 2, wherein said photodiode sidewall is disposed substantially perpendicular with respect to a surface of a substrate on which said pixel array is disposed.

4. A solid state imager as recited in Claim 1, 2 or 3 wherein said field plate is disposed over the substantially perpendicular portion of said photodiode sidewall.

5. A method of fabricating an imager array having a plurality of pixels, each pixel comprising a respective pixel thin film transistor and a pixel photosensor, the method comprising, for each respective pixel, the steps of:

   depositing a first conductive layer on a substrate;
   forming a photosensor bottom electrode from said first conductive layer;
   forming a photosensor body disposed on at least a portion of said photosensor bottom electrode, said photosensor body having sidewalls;
   depositing a gate electrode dielectric layer over said photosensor body;
   forming a layer of field plate comprising amorphous silicon on at least a portion of said gate dielectric layer covering said sidewall of said photosensor body and extending completely around said photosensor body; and
   forming a common electrode in electrical contact with said field plate.

6. The method of Claim 5, wherein the step of forming said common electrode further comprises:

   depositing a source/drain conductive material;
   patterning said source/drain conductive material to form said common electrode and to form a source electrode and a drain electrode for a thin film transistor (TFT) for each of said pixels.

7. The method of Claim 5 or 6, further comprising the step of forming an island of TFT material following deposition of said gate electrode dielectric layer, comprising the steps of:

   depositing a first layer of intrinsic amorphous silicon over substantially an entire exposed surface of said gate dielectric material;
   depositing a second layer of n^+-doped amorphous silicon material over said layer of intrinsic amorphous silicon; and
   etching said first and second layers to substantially remove said first and second layers from predetermined portions of said gate dielectric layer disposed so as to leave said first and second layers in selected area where said TFT islands are to be present, and further leaving intact at least a portion of said first layer of amorphous silicon on said sidewall of said photosensor body.

8. A radiation imager comprising:

   a substrate;
   a photosensor array disposed on said substrate, said photosensor array comprising a plurality of pixels, each of said pixels being coupled to a scan line and a data line, each of said pixels further comprising:

a photodiode having a body with sidewalls;
a thin film transistor (TFT), said TFT being electrically coupled to said photodiode and said scan line and data line so as to enable selectiv readout of the charge of said photodiode;
a common electrode disposed in electrical contact with said photodiodes; and

a field belt comprising amorphous silicon disposed around said photodiod sidewalls with a dielectric material being disposed between said field plate and said photodiode body, said field belt being in electrical contact with said common electrode so as to provide an electric field around said photodiode body in correspondence with the potential of said common electrode.

9. The radiation imager of claim 8 wherein said common electrode, at points where it is disposed over the sidewalls of said photodiode bodies, is disposed over respective TFT islands, said TFT islands comprising silicon materials used in the TFT fabrication process.

10. The radiation imager of claim 8 or 9 wherein said photodiode body sidewalls over which said field plate extends comprise a portion that is substantially vertical to the surface of said substrate.

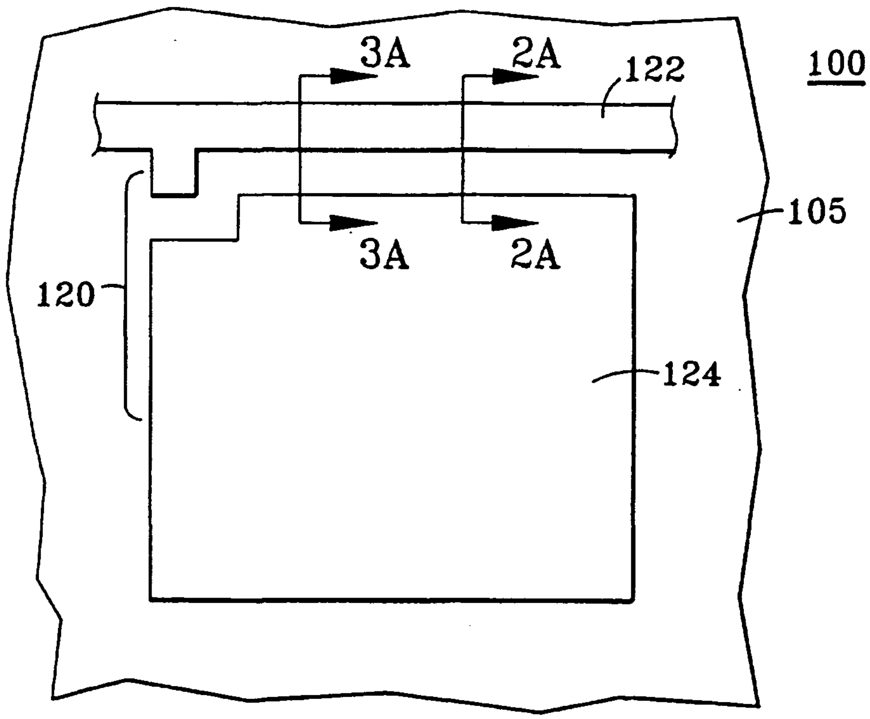

FIG. 1A

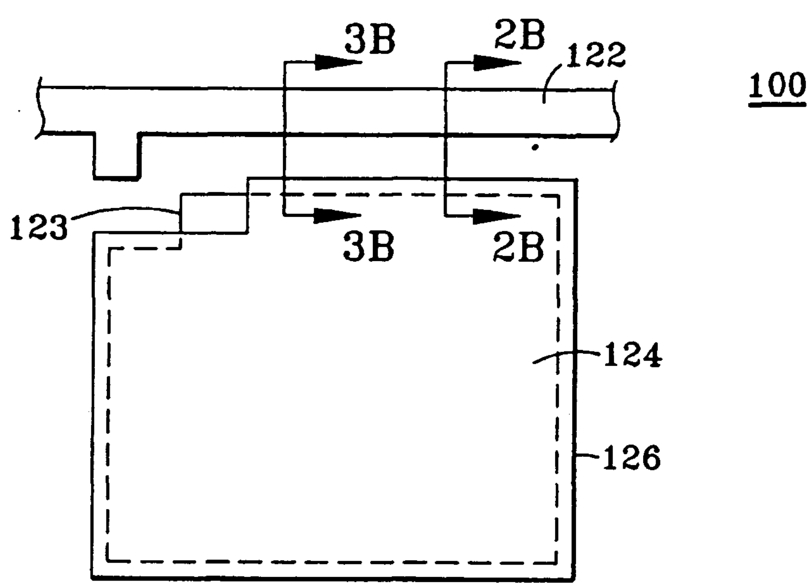

FIG. 1B

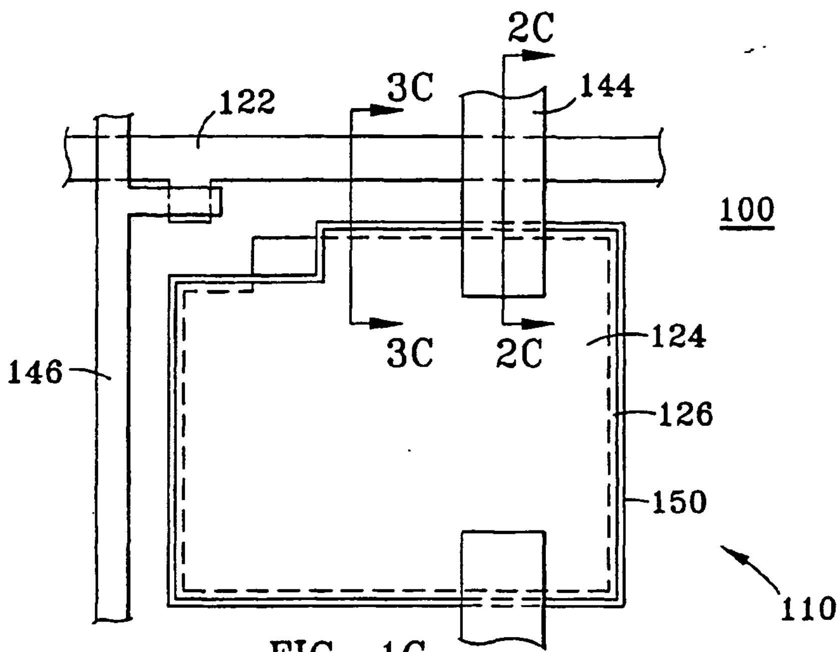
2C
3C
122
144
100
146
124
126
150
110
3C
2C

FIG. 1C

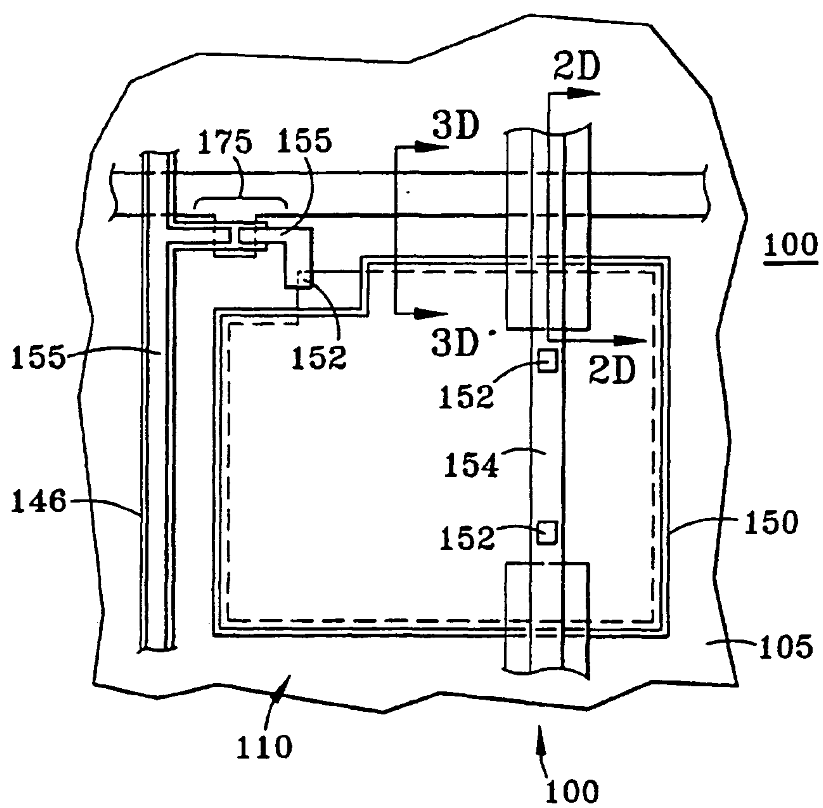
2D
3D
175
155
100
155
152
3D
2D
152
154
146
152
150
105
110
100

FIG. 1D

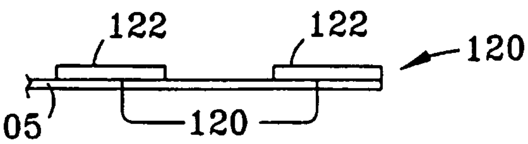

FIG. 2A

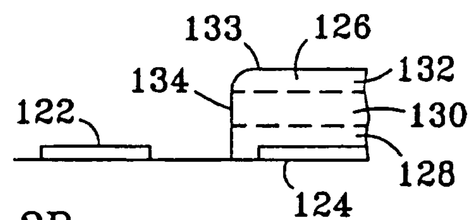

FIG. 2B

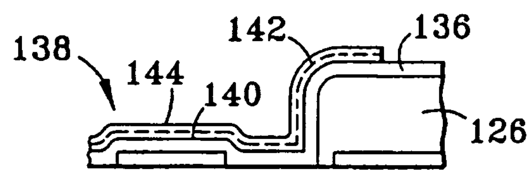

FIG. 2C

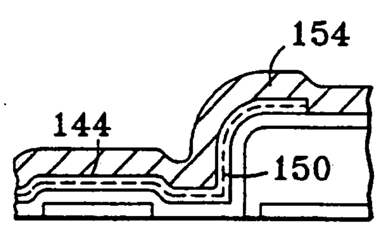

FIG. 2D

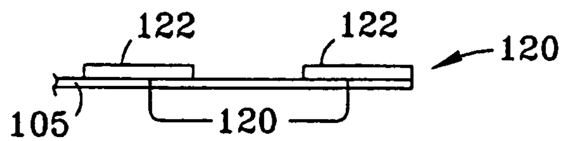

FIG. 3A

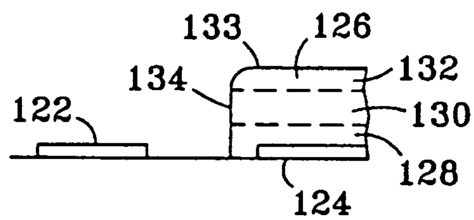

FIG. 3B

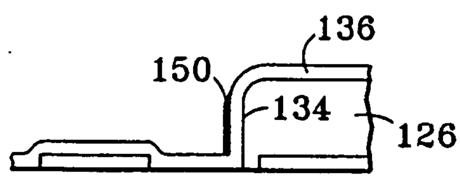

FIG. 3C

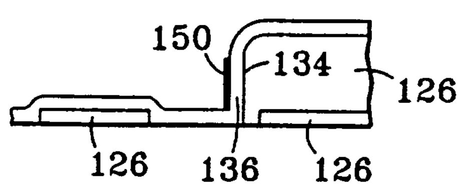

FIG. 3D

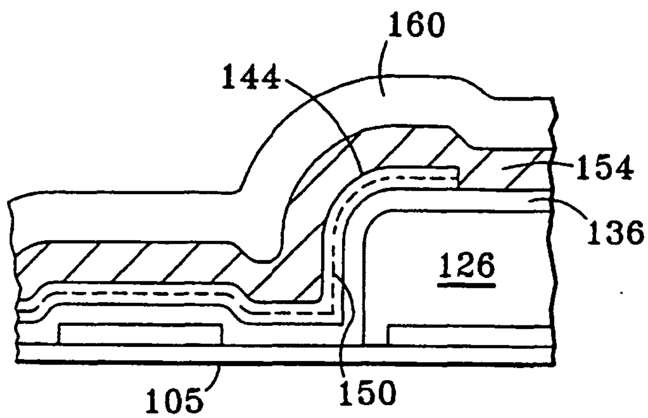

FIG. 4

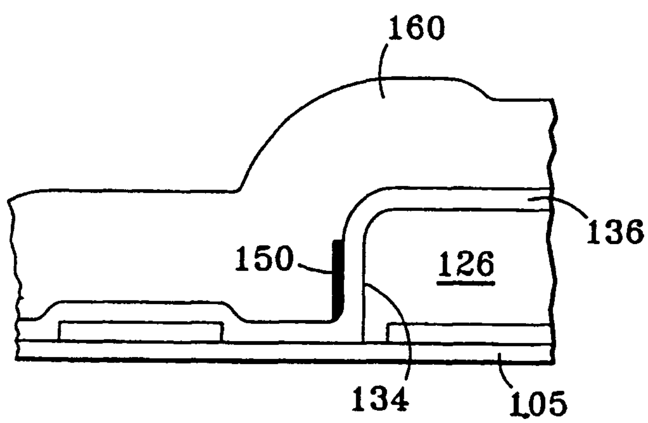

FIG. 5

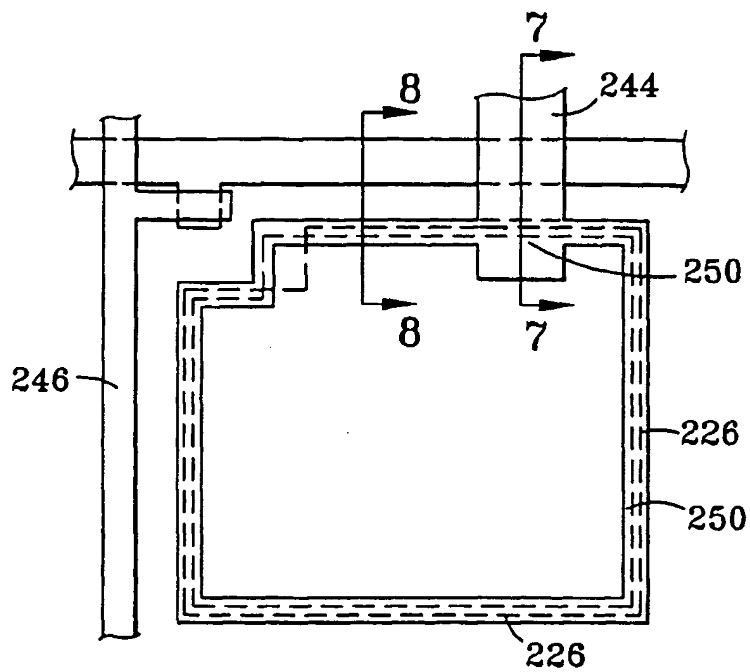

FIG. 6

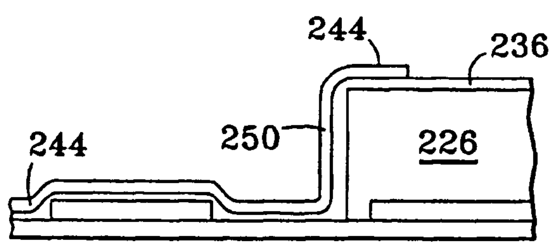

FIG. 7

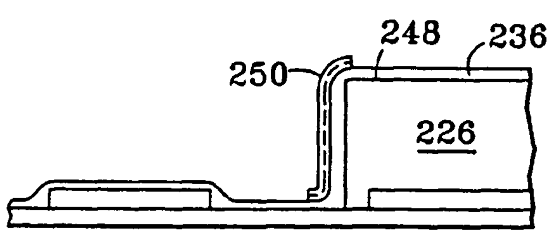

FIG. 8

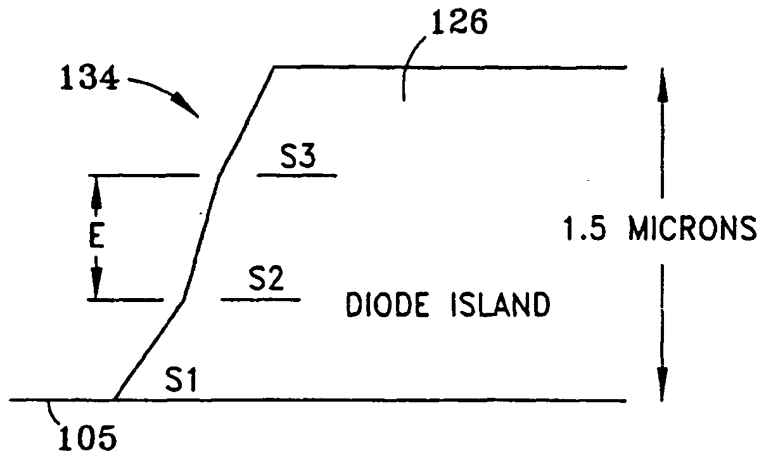
126
134
S3
E
1.5 MICRONS
S2
DIODE ISLAND
S1
105

FIG. 9

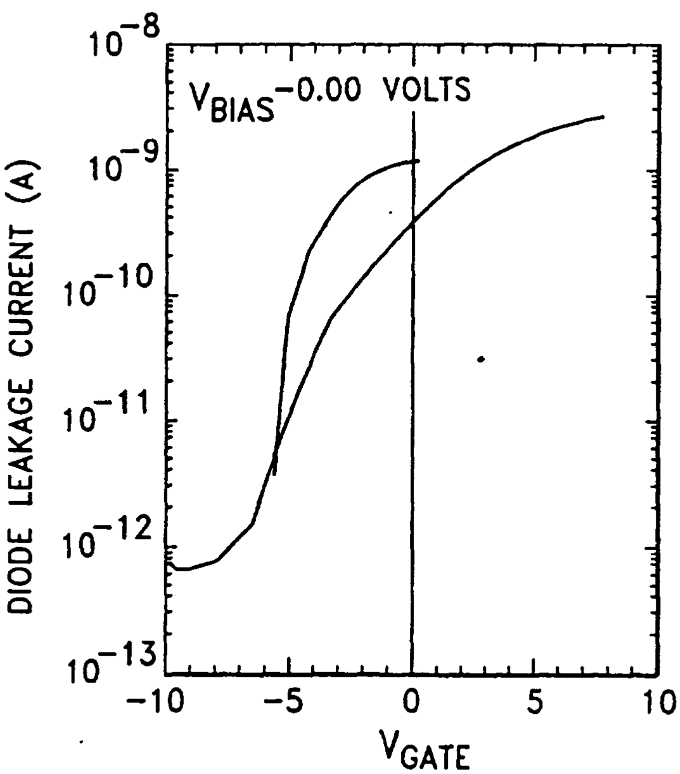
10^{-8}
V_{BIAS}-0.00 VOLTS
10^{-9}
10^{-10}
10^{-11}
10^{-12}
10^{-13}
DIODE LEAKAGE CURRENT (A)
-10
-5
0
5
10
V_{GATE}

FIG. 10

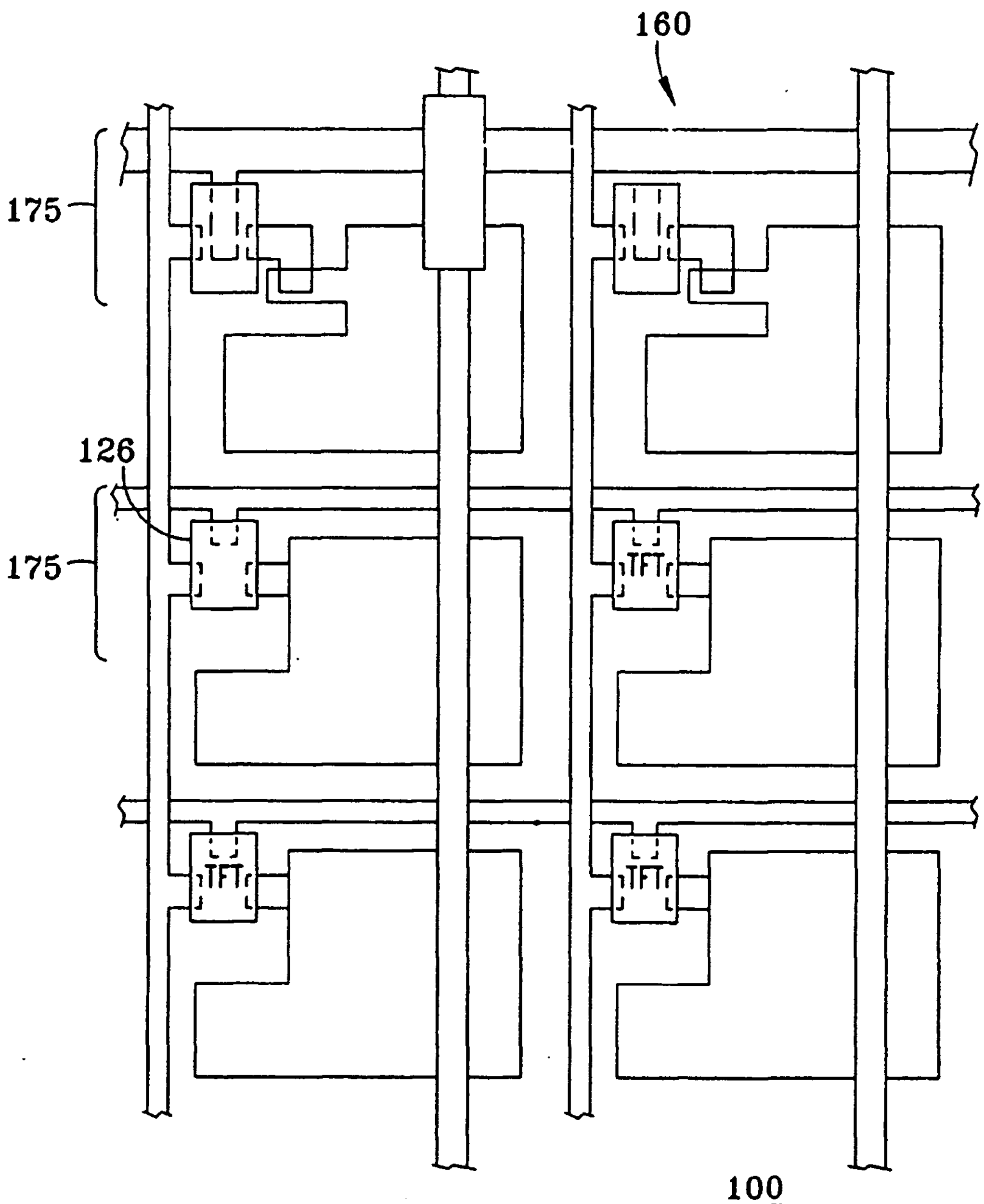

FIG. 11